Research Accelerator for Multiple Processors

RDL: Applications & Advanced Uses

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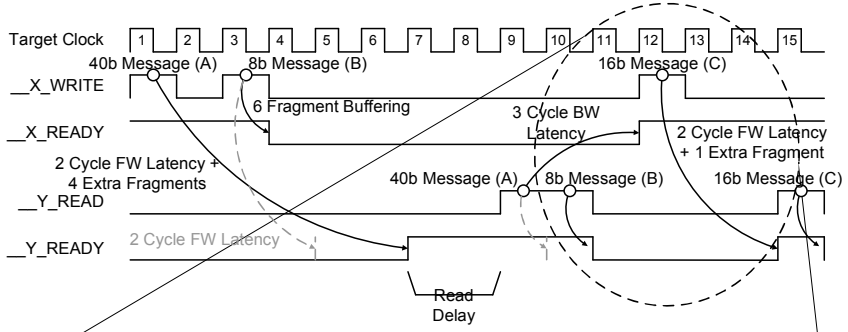
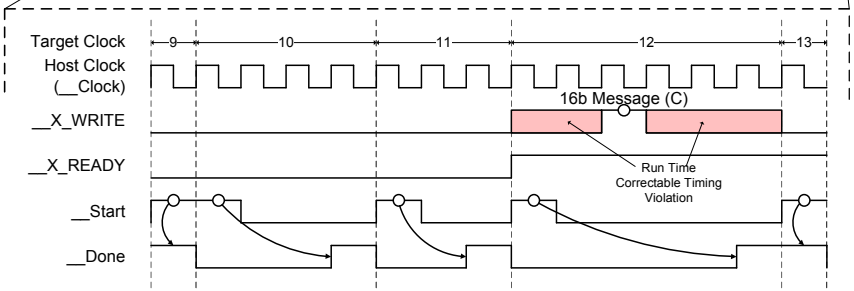
Channel Timing

- Bitwidth
  Size of fragments
  Bits/Fragment
- FW Latency
  Latency for data
  Target Cycles
- Buffering
  Channel capacity
  # of Framents
- BW Latency
  Latency for ACK
  Target Cycles

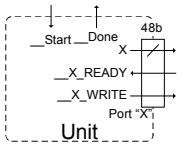


Target Level Timing Example - Channel <8, 2, 6, 3>

Virtualization of Time



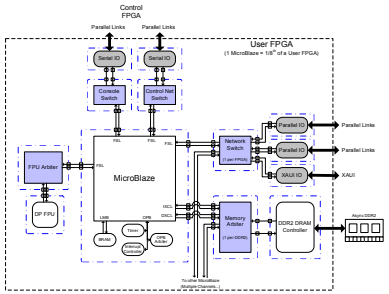
Host Level Timing Example



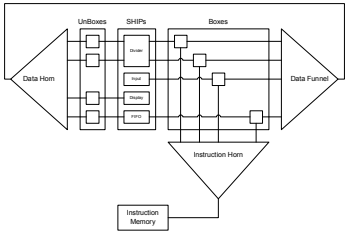
Sending Unit

- Start & Done
  Regulate the length of a target cycle, virtual, with respect to the host, physical, clock.
- Simulation of Timing & Latency
  Automatic "token" message fragments or timestamps could be used to indicate of a target cycle.

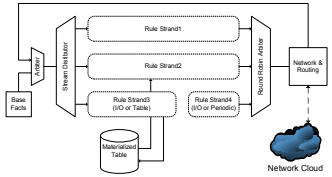
Applying RDL



RAMP Blue

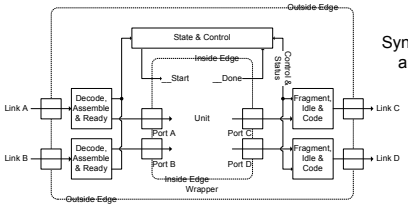


FLEET



P2/Overlog

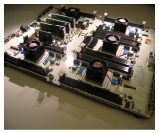
RDLC Map (Plugins)

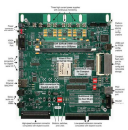


- **Complete host implementation**
- **Includes auto-generated units**

Synthesis, PAR and BitGen

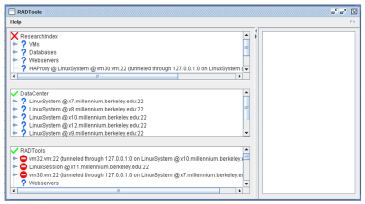
BEE2

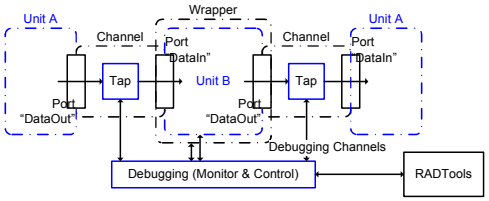




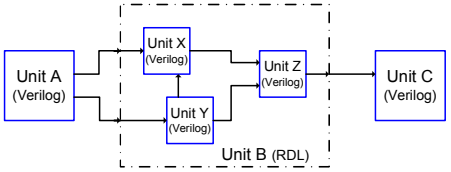
Xilinx XUP

Debugging

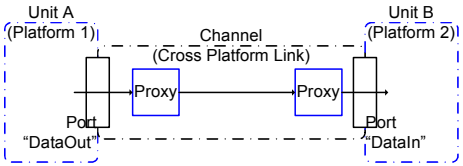




Advanced Uses of RDL



RDL in RDL



Zero Delay Channels (Link Built in RDL)